REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By the foregoing amendments, claims 1 and 2 have been amended. Claims 25-28 have been previously canceled, and claims 5-10 and 15-24 have been withdrawn. Thus, claims 1-4, 11-14 and 29-30 are currently pending in the application and subject to examination.

In the Office Action mailed November 2, 2005, claims 1, 4 and 20 were objected to for informalities. Claim 1 has been amended responsive to this objection, and the identifiers of claims 4 and 20 have been corrected. If any additional amendment is necessary to overcome this objection, the Examiner is requested to contact the Applicant's undersigned representative.

Claims 1-2 and 29-30 were rejected under 35 USC § 103(a) as being unpatentable over Maki (US 5,907,357) in view of Erstadt (US 6,356,101). Claims 11-14 were rejected under 35 USC § 103(a) as being unpatentable over Maki in view of Erstadt and further in view of Fuji (US 5,768,203). It is noted that claims 1 and 2 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicant hereby traverses the rejections, as follows.

As disclosed in the specification as filed, at, for example, p. 12, line 33 – p. 13, line 17, the CMOS sensor circuit of the claimed invention is characterized by a transistor, e.g., M5, that is provided to control a blooming of the CMOS sensor circuit. In the CMOS sensor circuit of FIGS. 4A and 7, for example, when the reset control signal Vrs changes from a low level to a high level, the transistor M4 is set in an OFF

state and the transistor M6 is set in an ON state. At this time, the node of the reset signal RST comes to have a potential near the threshold voltage Vth of the transistor M5, and this potential is applied to the gate of the reset transistor M1. The reset transistor M1 is turned ON, and an excessive amount of electric charge accumulated in the photodiode PD can escape to the terminal of the reset voltage source VR via the reset transistor M1 to restrain the blooming. The delay circuit is provided to produce the first signal by delaying the second signal, and the purpose of the delay circuit is to shorten the time for clamping the reset voltage, and enable the charge from the PD to escape to the terminal of the reset voltage source VR via the reset transistor earlier.

Maki teaches a charge transfer device using a switching circuit. The device of Maki is directed to controlling the reset gate for charge transfer in a CCD sensor. However, Maki does not disclose or suggest at least the combination of an inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit, as recited in claims 1 and 2, as amended.

Erstad was cited to show a glitch removal circuit for removing glitches from an inverter circuit using a delay line. However, Erstad does not disclose or suggest at least the combination of an inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of

the CMOS sensor circuit, as recited in claims 1 and 2, as amended.

Fuji was cited as allegedly disclosing some features of dependent claims 11-14 of the subject application. However, Fuji does not disclose or suggest at least the combination of an inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit, as recited in claims 1 and 2, as amended.

Therefore, the Applicants respectfully submit that none of the cited art of record, nor combination thereof, discloses or suggests at least the combination of a voltage control circuit controlling a gate potential of said reset transistor to a potential other than power source potentials, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit, as recited in claims 1 and 2, as amended.

For at least this reason, the Applicants submit that claims 1 and 2, as amended, are allowable over the cited art of record. As claims 1 and 2 are allowable, the Applicants submit that claims 3-4, 11-14 and 29-30, each of which depends from one of allowable claims 1 and 2, are likewise allowable.

Conclusion

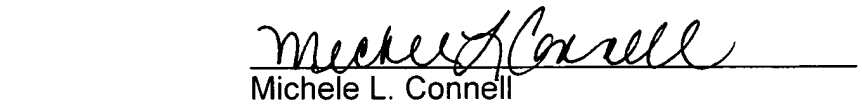
For all of the above reasons, it is respectfully submitted that the claims currently pending are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100353-00095.

Respectfully submitted,

Arent Fox, PLLC



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